Shri Shankaracharya Technical Campus,

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SCHEME OF TEACHING AND EXAMINATION

Courses of Study and Scheme of Examination of M. Tech

2nd Semester M. Tech. Electronics & Telecommunication (VLSI Design)

S. No.	Board of Study	Subject Code	Subject	Periods per week			Scheme of Exam Theory/Practical			Total Marks	Credit L+(T+P)/2
				L	T	P	ESE	CT	TA		
1.	Electronics & Telecom	ET231201	Digital Logic with Verilog Design	3	1	-	100	20	20	140	4
2.	Electronics & Telecom	ET231202	VLSI System Testing	3	1	-	100	20	20	140	4
3.	Electronics & Telecom	ET231203	Low Power VLSI Design	3	1	-	100	20	20	140	4
4.	Electronics & Telecom	ET231204	Embedded System Design	3	1	-	100	20	20	140	4
5.	Electronics & Telecom	Refer Table II	Elective – II	3	1	-	100	20	20	140	4
6.	Electronics & Telecom	ET231291	Verilog Design and verification Lab	-		3	75		75	150	2
7.	Electronics & Telecom	ET231292	Embedded system Lab	-		3	75		75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table II

Elective-II			
Sr.No.	**Board of Study**	**Subject Code**	**Subject**
1	Electronics & Telecom	ET231221	MEMS and IC integration
2	Electronics & Telecom	ET231222	MOS Physics
3	Electronics & Telecom	ET231223	Neural Network for VLSI

L-Lecture T- Tutorial P-Practical
CT- Class Test TA- Teachers Assessment ESE- End Semester Exam

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SCHEME OF EXAMINATION AND SYLLABUS

2nd SemisterM.Tech. Electronics & Telecommunication (VLSI Design)

Subject Code :- ET231201	**Digital Logic with Verilog Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand **the computer added design tool and design various arithmetic and multilevels circuits and analysis its parameters** for optimization of circuits	On successful completion of the course, the student will be able to: **CO1:-**work on Computer added Design tool and implement Various digital Structure. CO2:-learn various Implementation Technology of Mixed Circuits **CO3:-**Understand the technique through which they can optimize the logic Function. **CO4**:-Design Various arithmetic Circuit in Computer added Design tool. **CO5:-**Design Various Combinational and Sequential Circuit Implementation

UNIT-I: Introduction to logic circuits: **CO1**

Variables and functions, Sysnthesis using AND, OR and NOT gates, Introduction to CAD tools, Introduction to Verilog**[5Hrs]**

UNIT–II :Implementation Technology: **CO2**

Transistor switches, CMOS Logic, PLD, Transmission gates**[5Hrs]**

UNIT – III : Optimized Implementation of Logic Function : **CO3**

Strategy for minimization ,minimzation of POS, Multiple Output circuits, Analysis of Multilevel Circuits**[5Hrs]**

UNIT – IV : Number Representation and Arithmetic Circuits **CO4**

Positional Number representation, Addition of unsigned numbers, signed Numbers, Fast adders, Design of arithmetic circuits using CAD tools, Multiplication.**[5Hrs]**

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UNIT – V : Combinational Circuit Building blocks: **CO5**

Multiplexers, Decoder, Encoder, Code Converters, Arithmetic Comparison circuits, Verilog for combinational circuits Design of Sequential design, Design Asynchronous Sequential Design. **[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Fundamental of digital Logic with Verilog design	S. Brown & Z. Vransesic	Third	TMH
2	Verilog primer	J.Bhasker	Eight	Pearson education

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Fundamental of digital Logic with Verilog design	S. Brown & Z. Vransesic	Third	TMH
2	Verilog primer	J.Bhasker	Eight	Pearson education

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2nd Semester M.Tech. Electronics & Telecommunication (VLSI DESIGN)

Subject Code ET231202	VLSI System Testing	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The aim is to To expose the students, the basics of testing techniques for VLSI circuits and Test Economics	On successful completion of the course, the student will be able to: **CO1:-**apply the concepts in testing which can help them design a better yield in IC design **CO2:-**tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs **CO3**. identify the design for testability methods for combinational & sequential CMOS circuits **CO4:-**analyse the various test generation methods for static & dynamic CMOS circuits**.** **CO5:-** recognize the Silicon Debug Principles for improving testability.

UNIT-I: SPECIAL PURPOSE SUBSYSTEMS: **CO1**

Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc. **Design Economics**: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example**[5Hrs]**

UNIT – II : TESTING OF COMBINATIONAL CIRCUITS: **CO2**

circuits – Failures and faults – Modeling of faults – Temporary faults – Test generation for Combinational logic circuits – testable combinational logic circuit design – Scan based design and JTAG testing issues**[5Hrs]**

UNIT – III: TESTING OF SEQUENTIAL CIRCUITS **CO3**

Test generation for sequential circuits – Design of testable sequential CK5- Built in self test – Testable memory design.**[5Hrs]**

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UNIT – IV: VERIFICATION AND TESTING **CO4**

Verification – Timing verification – Testing concepts – Fault coverage – ATPG – Types of tests – Testing FPGAs – Design for testability.**[5Hrs]**

UNIT – V: VLSI SYSTEM TESTING & VERIFICATION **CO5**

Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan. VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.**[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	"CMOS VLSI Design: A Circuits and system perspectives	Neil H.E. Weste, Davir Harris	3rd Edition	Pearson Education
2	Modern VLSI design: System on Silicon	Wayne, Walf	Second Edition	Pearson Education
3	"Digital System Testing and Testable Design",	M. Abramovici, M. A. Breuer, & A.D. Friedman	Second Edition	Computer Science Press

ReferenceBooks:

S. No.	Title	Authors	Edition	Publisher
1	"Basic VLSI Design	Pucknull	3rd Edition	PHI
2	Digital circuit Testing and Testability	P. K. Lala	2nd Edition	Academic Press.

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2nd Semester M.Tech. Electronics & Telecommunication(VLSI Design)

Subject Code :- ET231203	**Low Power VLSI Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand **the computer added design tool and design various arithmetic and multilevels circuits and analysis its parameters** for optimization of circuits	On successful completion of the course, the student will be able to: CO1:-Understand the Technology advancement and its impact on Power Consumption of Circuit. CO2:-learn Power estimation Simulation and different Power analysis techniques CO3:-Design the power Optimized Sequential Circuit and its Analysis. CO4:-Understand Low power Architecture & Systems CO5:-Design the Clock Based Circuit and Check the Impact of timing on Ciruit.

UNIT-I: Device& Technology Impact on Low Power : **CO1**

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Lowpower approaches. Physics of power dissipation in CMOS devices. Dynamic dissipation in CMOS, Transistorsizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. **[5Hrs]**

UNIT–II : Power estimation Simulation Power analysis: **CO2**

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.**[5Hrs]**

UNIT – III : Low Power Design Circuit level: **CO3**

Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic**[5Hrs]**

UNIT – IV : Low power Architecture & Systems: **CO4**

Power & performance management, switching activity reduction, parallel architecture with voltage reduction,

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flow graph transformation, low power arithmetic components, low power memory design.**[5Hrs]**

UNIT – V: Low power Clock Distribution: **CO5**

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network Algorithm & architectural level methodologies : Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.**[5Hrs]**

Text Books:

S.No.	Title	Authors	Edition	Publisher
1	"Practical Low Power Digital VLSI Design"	Gary K. Yeap	Third	KAP, 2002
2	"Low power design methodologies"	Rabaey, Pedram	Eight	Kluwer Academic, 1997

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	"Low-Power CMOS VLSI Circuit Design"	Kaushik Roy, Sharat Prasad	Third	Wiley, 2000

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SCHEME OF EXAMINATION AND SYLLABUS

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Subject Code ET231204	**Embedded System Design**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
To make students familiar with the basic concepts and terminology of the embedded systems design flow. – To give students an understanding of the embedded system architecture and software development tools.	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of Embedded Hardware. **CO2:-**Understand PIC Microcontroller and their interfacing. **CO3:-**understand concept of different Microcomputer and their interfacing concepts. **CO4:-**Design embedded system using software and tools. **CO5:-**Learn to task, data and memory management in real time operating system.

UNIT-I: REVIEW OF EMBEDDED HARDWARE **CO1**

Terminology Gates - Timing Diagram - Memory - microprocessors Buses-Direct Memory Access-interrupts - Built-ins on the Microprocessor-Conventions Used on Schematic-schematic. Interrupts Microprocessor Architecture-Interrupt Basics-Shared Data Problem-Interrupt latency. **[5Hrs]**

UNIT – II: PIC MICROCONTROLLER AND INTERFACING **CO2**

Introduction, CPU architecture, registers, instruction sets addressing modes Loop timing, timers, Interrupts, Interrupt timing, I/o Expansion, I 2C Bus Operation Serial EEPROM, Analog to digital converter, UART-Baud Rate-Data Handling-Initialisation, Special Features - serial Programming-Parallel Slave Port. **[4Hrs]**

UNIT – III : EMBEDDED MICROCOMPUTER SYSTEMS **CO3**

Motorola MC68H11 Family Architecture Registers, Addressing modes Programs. Interfacing methods parallel I/O interface, Parallel Port interfaces, Memory Interfacing, High Speed I/o Interfacing, Interrupts-interrupt service routine-features of interrupts-Interrupt vector and Priority, timing generation and measurements, Input capture, Output compare, Frequency Measurement, Serial I/o devices Rs.232, Rs.485. Analog Interfacing, Applications. **[5Hrs]**

UNIT – IV: SOFTWARE DEVELOPMENT AND TOOLS **CO4**

Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Intergrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies,Simulators.**[5Hrs]**

UNIT – V: REAL TIME OPERATING SYSTEMS **CO5**

Task and Task States, tasks and data, semaphores and shared Data Operating system Services - Message queues- Timer Function-Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.**[5Hrs]**

Text Books:

S.No	Title	Authors	Edition	Publisher
1	An embedded software primer	David E Simon	2001	Pearson education Asia
2	Design with Microcontroller	John B Peat man	1998	Pearson education Asia
3	Embedded Micro computer Systems. Real time Interfacing	Jonartthan W. Valvano	2001	Thomson learning

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Real-Time Systems and Programming Languages	Burns, Alan and Wellings, Andy	1997	Addison-Wesley-Longman
2	An Introduction to real time systems: Design to networking with C/C++	Raymond J.A. Bhur and Donald L.Bialey	1999	Prentice Hall Inc. New Jersey
3	Real time Programming: A guide to 32 Bit Embedded Development. Reading	Grehan Moore, and Cyliax	1998	Addison-Wesley-Longman
4	Embedded Systems Design	Heath, Steve	1999	Newnes

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2nd Semester M.Tech. Electronics & Telecommunication (VLSI DESIGN)

Subject Code ET231221	**MEMS and IC Integration**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
To make students familiar with the basic concepts and terminology of the MEMS and IC Integration. – To give students an understanding of the MEMS and IC Integration.	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of MEMS and IC Integration. **CO2:-**Understand layer Formation process and PVD. **CO3:-**Understand concept of lithography and their concepts. **CO4:-** Understand Micro stereo lithography for MEMS. **CO5:-** Understand the Micro sensors.

UNIT-I **CO1**

Introduction, Evolution of Microsensors and MEMS, micrometallurgy and material characterization, microscopy and visualization, lateral and vertical dimensions, electrical measurements, physical and chemical analysis, XRD, TXRF, SIMS, AES, XPS, RBS, EMPA, analysis area and depth

UNIT-II **CO2**

Silicon material properties, crystal growth, crystal structure, wafer process, Thin Film Material and Process: PVD and CVD, Metallic thin films and Dielectric thin films, properties of dielectric film, Epitaxy, Thin Film Growth and Structure: PVD and CVD film growth and structure.

UNIT-III **CO3**

Pattern generation, optical lithography, lithographic patterns, etching: wet etching, electromechanical etching, anistropic wet etching, plasma etching, wafer cleaning and surface preparation.

UNIT-IV **CO4**

Micro stereo lithography for MEMS: Photo polymerization , stereo lithographic system, micro stereo lithography , scanning methods, two photon MSL, other MSL approaches, Polymeric MEMS architecture with silicon, metal and ceramics, combined structure and applications RF MEMS, and Optical MEMS

UNIT-V **CO5**

Micro sensors: Thermal sensors, Radiation Sensors, magnetic sensors, Biochemical sensors, Introduction to SAW Devices, MEMS-IDT Micro sensors: Principle, fabrication, testing wireless readout, hybrid accerolometers and gyroscope.

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Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Introduction to Microfabrication	Sami Franssila	2nd	John Wiley
2	Microsensors MEMS and Smart Devices	Gardner	2013	John wiley

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Microactuators	Masood Tabib-Azar	1998	Kluwer
2	Sensor Technology and Devices,	Ljubisa Ristic	1994	Artech House Cambridge

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SCHEME OF EXAMINATION AND SYLLABUS

2nd Semester M.Tech. Electronics & Telecommunication (VLSI DESIGN)

Subject Code ET23122	**MOS Physics**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
To make students familiar with the basic concepts and terminology of the MOS Physics flow. – To give students an understanding of the MOS Physics .	On successful completion of the course, the student will be able to: **CO1:-**Outline the features of MOS Device Physics. **CO2:-**Understand Small-Geometry Effects. **CO3:-**understand concept of different MOS IC Processes. **CO4:-**Design MOS Digital IC using different designing technique. **CO5:-**Learn to Analog MOS Design.

UNIT-I **CO1**

MOS Device Physics: Triode Region, Saturation Region, Avalanche Region, Sub threshold Region, Second Order Effects, Ways of Measuring Threshold Voltage, MOS Device Applications.

UNIT –II **CO2**

Small-Geometry Effects: Nonuniform doping & Effect on Threshold voltage, Sub tThreshold current, Short-channel effect, Narrow width effect, Small-Geometry effects, Shrink & Scaling, Scaling down the Dimensions of MOS Devices.

UNIT –III **CO3**

MOS IC Processes: Metal Gate PMOS, The Hypothetical Metal-Gate NMOS, Metal-Gate CMOS, Silicon Gate LOCOS NMOS Processes, The HMOS Process, Process Enhancements.

UNIT-IV **CO4**

MOS Digital IC Design: Building Blocks for MOS digital IC, Inverter DC Analysis, Inverter Transient Analysis, MOS Logic Circuits, Memory Circuits, Other Circuit Techniques.

UNIT-V **CO5**

Analog MOS Design: Considerations in Analog MOS circuits, Analog Building Blcoks, MOS Operational Amplifiers, Capacitor Based Circuits, Switched Capacitor Filters, Charge Coupled Devices, Charge Coupled Device Applications

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Text Books:

S.No.	Title	Authors	Edition	Publisher
1	Modern MOS Technolgy: Processes, Devices and Design	DeWitt G. Ong	2nd	McGraw Hill Book Co.
2	Security in Computing	Charels P. Pfleeger	2014	Prentice Hall

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Inside Internet Security	Jeff Crume	-	Addison Wesley

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SCHEME OF EXAMINATION AND SYLLABUS

2nd Semister M.Tech. Electronics & Telecommunication (VLSI DESIGN)

Subject Code ET231223	**Neural Network for VLSI**	**L = 3**	**T = 1**	**P = 0**	**Credits = 4**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**ESE Duration**
	100	**20**	**20**	**140**	**3 Hours**

Course Objective	**Course Outcomes**
The objective is to make the students understand and conceptualize the basics of **Artificial Neural Network architecture**. The aim is to impart skills to students for developing and hosting Neural Network circuit establishment.	On successful completion of the course, the student will be able to: **CO1:-** Understand the Basic introduction of neural network. **CO2:-** Learn artificial neural network and learning rule. **CO3:-** Understand the Supervised Learning and Neurodynamics. **CO4:-** Understand the Design Unsupervised and Hybrid Learning. **CO5:-**Learn the Applications for VLSI Design. .

UNIT- I Introduction: **CO1**

Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons. **[5Hrs]**

UNIT–II ANN architecture: **CO2**

Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning. **[5Hrs]**

UNIT – III Supervised Learning and Neurodynamics: **CO3**

Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories. **[5Hrs]**

UNIT – IV **CO4**

Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ART networks, LVQ **[5Hrs]**

UNIT – V **CO5**

Applications for VLSI Design: Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting. **[5Hrs]**

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Text Books:

S.No.	Title	Authors	Edition	Publisher
1	An Introduction to Neural Networks	Anderson J.A.	1999	PHI
2	Neural Networks-A Comprehensive Foundations	Haykin S	1999	Prentice-Hall International, New Jersey

Reference Books:

S. No.	Title	Authors	Edition	Publisher
1	Neural Networks: Algorithms, Applications and Programming Techniques	Freeman J.A., D.M. Skapura	1992	Addison-Wesley, Reading, Mass
2	Mathematical Methods for Neural Network Analysis and Design	Golden R.M	1996	MIT Press, Cambridge

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Subject Code ET231291	**Verilog Design and Verification Lab**	**L = 0**	**T = 1**	**P = 2**	**Credits = 2**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**Lab Periods**
	75	**20**	**75**	**150**	**10**

List of experiments to be performed:

1. 8 bit shift register

2. 8:1 multiplexer

3. Barrel shifter

4. N by m binary multiplier

5. RISC CPU (3bit opcode, 5bit address)

6. SPICE simulation of basic analog circuits.

7. Verification of layouts (DRC, LVS)

Tools used : Cadence tools, Mentor Graphics tools, lab view tools, multisim, SILVACO

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Subject Code ET231292	**Embedded System Lab**	**L = 0**	**T = 1**	**P = 2**	**Credits = 2**
Evaluation Scheme	**ESE**	**CT**	**TA**	**Total**	**Lab Periods**
	75	**20**	**75**	**150**	**10**

List of experiments to be performed:

(i) Create ,compile and test a program to print a string a message on standard output device

(ii) Create a program to print powers of 2 from 20 to 212

(iii) Write a program tht continuously reads Port A and provides output to port B

(iv) Use External Hard ware Interrupt to print a message to the standard output devices each time an interrupt occurs . Also print number of time interrupt occur

(v) Create a program that will turn on an LED when falling edge occur on external interrupt 0 and turn it off when rising edge occour on external interrupt 1

(vi) Create a programme that will demonstrate how watchdog timer resets the processor if programme hangs up to infinite loop

(vii) Create a programme that will read the data on all 8 bits of port B swap the nibble of data and send it to port A

(viii) Create a simulated engine speed monitor that will light a LED if the motor speed drops below 200rpm and another LED if motor speed exceed 500 rpm and light another LED if motor speed between 200 to 500 rpm

(ix) Create a programme to output the ASCII character G every 50 msec via USART at 9600 baud rate

(x) Write a microcontroller 8051 program to add two floating-point numbers.

(xi) Write a microcontroller 8051 program to multiply two floating-point numbers.

(xii) Write a microcontroller 8051 program that generates 2kHz square wave on pin P1.0, 2.5 kHz on pin P1.2 and 25 Hz on pin P1.3.

(xiii) Write a microcontroller 8051 program for counter 1 in mode 2 to count the pulses and display the state o the TL1 count on P2. Assume that the clock pulses are fed to pin T1.

(xiv) Write a microcontroller 8051 program to transfer word “COMMUNICATION” serially at 4800 baud and one stop bit, to the com port of PC continuously.

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(xv) Write a microcontroller 8051 program to receive bytes of data serially, and put them in P1. Set the baud rate at 2400 baud, 8-bit data, and 1 stop bit. Assume crystal frequency to be 11.0592 MHz.

Recommended Books:

1. Embedded C Programming and the Microchip by PIC Barneet , Cox ,O'cull
Thomson publication
2 Embedded system by Raj Kamal TMH

List of Equipments/Machine Required :

1. MATLAB Software with Simulink
2. Emulation software with Cross C complier